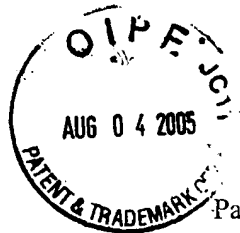


10/642,201.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentees: Joo-Sun YOON, *et al.*

Issued: March 1, 2005

Patent No.: US 6,862,060 B2

For: **TRANSFLECTIVE LIQUID CRYSTAL DISPLAY**

Attn: **CERTIFICATE OF CORRECTION BRANCH**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Certificate
AUG 15 2005
of Correction

REQUEST FOR CERTIFICATE OF CORRECTION
UNDER 37 C.F.R. 1.323
APPLICANT'S MISTAKE

Sir:

Transmitted herewith in duplicate is PTO Form 1050 - Certificate of Correction for the above-identified U.S. Patent correcting the Applicant's mistake as shown in the enclosed Certificate of Correction form. Also attached is a copy of the relevant page of the Letters Patent, with the requested correction marked in red ink.

Issuance of a Certificate of Correction is in order. Since this matter was incorrectly shown on the Specification filed August 18, 2003 with the U.S. Patent and Trademark Office, and involves a minor diction error, our check in the amount of \$100.00 is submitted herewith.

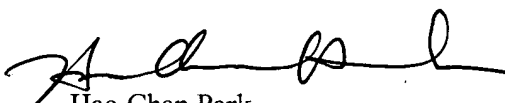
Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account No. 23-1951.

Respectfully submitted,

08/05/2005 SSITHIB1 00000056 6862060

01 FC:1811

100.00 OP


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AUG 16 2005

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.: 6,862,060 B2
DATED: March 1, 2005
INVENTORS: Joo-Sun YOON, *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below.

At column 8, line 15, please delete "second" and insert -- first --

At column 8, line 19, please delete "first" and insert -- second --

MAILING ADDRESS OF SENDER:

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PATENT NO.: 6,862,060 B2
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FORM PTO 1050 (Rev. 2-93)

AUG 16 2005

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mounted on the gate TCPs 400 and the data TCPs 500, respectively. A plurality of leads (not shown) connected between the gate driving ICs 410 and the signal path 451 and between the gate driving ICs and the gate lines 121 are formed on the gate TCPs 410. Another plurality of leads (not shown) connected between the data driving ICs 510 and the signal paths 551 and 552 and between the data driving ICs 510 and the data lines 171 and 172 are formed on the data TCPs 500. Reference numerals 520 and 521 shown in FIG. 1 indicate the leads for transmitting signals for the dummy data lines 172, which are connected to the signal path 552.

The gate TCPs 400 and the data TCPs 500 are respectively attached to the gate PCB 450 and the data PCB 550 to be electrically connected thereto, and are attached to the panel assembly 300 to be electrically connected to the gate lines 121 and the data lines 171 and 172, respectively. Alternatively, the gate driving ICs 410 and/or the data driving ICs 510 are mounted on the TFT array panel 1, which is called a COG (chip on glass) type. Alternatively, the gate driving ICs 410 and/or the data driving ICs 510 are substituted with driving circuits formed in the TFT array panel 1, which are made of the same layers as the gate lines 121, the data lines 171 and 172 and the TFTs.

The LCD controller 700 provides a plurality of red, green and blue image signals for the data driving ICs 510 and a plurality of control signals for the driving ICs 410 and 510 via the signal paths 451, 551 and 552 on the PCBs 450 and 550 and the FPC film 600 to control the driving ICs 410 and 510. The gate driving ICs 410 generate the scanning signals based on the gate-on voltage and the gate-off voltage from the driving voltage generator 900 to apply to the gate lines 121 via the end portions 125 thereof in synchronization with the control signals from the LCD controller 700. The data driving ICs 510 select the gray voltages from the gray voltage generator based on the image signals from the LCD controller 700 to apply as the data signals to the appropriate data lines 171 and 172 via the end portions 179 thereof in synchronization with the control signals from the LCD controller 700.

In this LCD, the impurity ions on the surface of the aligning films 11 and 21 travel along the rubbing direction, and gather at the dummy pixel electrodes 195, in particular, near the lower right corner. As described above, since the dummy pixel electrodes 195 in the rightmost columns overlap the black matrix 220, the area with defect image caused by such ions is screened by the black matrix 220. Furthermore, the dummy pixel electrodes 195, which have no transmissive area, block the light from a light source. Accordingly, the LCD according to this embodiment compensates the defects in the dummy pixel areas DP.

According to another embodiment of the present invention, the rightmost regular pixel electrodes 190 are elongated along the gate lines 121 to overlap the black matrix 220 without providing the dummy pixel electrodes. The elongated portions of the pixel electrodes 190 have no transmissive area.

Although preferred embodiments of the present invention have been described in detail hereinabove, it shall be clearly understood that many embodiments having variations and/or

modifications of the basic inventive concepts herein taught are possible, which may appear to those of ordinary skill in the pertinent art based on the teachings herein. Such embodiments will fall within the spirit and scope of the present invention, as defined in the appended claims.

What is claimed is:

1. A liquid crystal display comprising:

a first insulating substrate including a display area and a peripheral area located outside the display area;

a plurality of signal lines provided on the first substrate;

a plurality of first pixel electrodes electrically connected to the signal lines and located in the display area, each first pixel electrode including a first transparent electrode and a ~~second~~ reflective electrode; and

a second pixel electrode electrically connected to the signal lines and located in the peripheral area, the second pixel electrode including a ~~first~~ transparent electrode and a second reflective electrode having an area larger than the first reflective electrode.

2. The liquid crystal display of claim 1, wherein the second reflective electrode covers substantially entire surface of the second transparent electrode.

3. The liquid crystal display of claim 2, wherein the first reflective electrode has a hole exposing a portion of the first transparent electrode.

4. The liquid crystal display of claim 1, further comprising:

a second insulating substrate disposed opposite the first substrate; and

a black matrix provided on the second substrate, the black matrix screening the second pixel electrodes.

5. The liquid crystal display of claim 4, further comprising a common electrode provided on the second substrate and disposed opposite the first and the second pixel electrodes, wherein the first and the second pixel electrodes and the common electrode are supplied with signals having periodically inverting polarity.

6. The liquid crystal display of claim 1, wherein the first and the second pixel electrodes are arranged in a matrix, the signal lines include a plurality of gate lines extending in a row direction and a plurality of data lines extending in a column direction, and the liquid crystal display further comprises a plurality of switching elements transmitting first signals from the data lines to the first and the second pixel electrodes in response to second signals from the gate lines.

7. The liquid crystal display of claim 6, further comprising an aligning film on the first substrate, wherein the aligning film is rubbed in a first direction toward the second pixel electrode.

8. The liquid crystal display of claim 7, wherein the first direction is oblique to the row direction and the column direction.

9. The liquid crystal display of claim 8, wherein each of the gate lines and the data lines has an end portion for signal communication with other device, and the first direction goes away from the end portions.

* * * * *